R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found on page 9, line 16 through page 10, line 5 and claims 5 and 7, as originally filed. No new matter has been added.

DRAWING OBJECTIONS

The objection to the drawings has been obviated by appropriate amendment to the claims and should be withdrawn.

EXAMINER'S ANALYSIS SECTION

Applicant's representative respectfully requests that the Examiner restrict comments in his Office Actions to the issues of the case. An analysis of Applicant's representative's writing style is not necessary to advance prosecution. For example, while the Examiner prefers run-on type sentences, Applicant's representative does not. However, there is no need to view the lack of a run-on construction as an overly broad interpretation. In particular, the Examiner's remarks about his computer are not relevant. The first circuit and the second circuit Applicant's representative describes are the first and second circuits as

claimed. The details of the claimed first circuit and the second circuit are in the very next sentence of text.

Furthermore, the Examiner's interpretation of analog signals having pixels is not entirely accurate on several levels. The Comprehensive Dictionary of Electrical Engineering defines a pixel as a "picture element" and each sample of a *digital image* (see attached Exhibit A). Pixels are digital in nature. While some (but not many) references refer to pixels in an analog sense, those references typically refer to a post A/D conversion.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5, 10, 11 and 22 under 35 U.S.C. §102(b) as being anticipated by Chen et al. has been obviated by appropriate amendment and should be withdrawn.

Chen discloses a list controlled video operations (Title).

In contrast, the present invention provides an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present an output signal having a first resolution and a plurality of output pixels in response to (i) an input signal having a second resolution and a plurality of input pixels and (ii) one or more control signals. The input signal is received a scan line at a time. The second circuit may be configured to generate the control signals in response to (i) a

previous calculation by the first circuit and (ii) one or more input parameters. The first circuit may be configured to scale and filter the input signal to allow one or more of the input pixels to contribute to the creation of one or more of the output pixels. The apparatus comprises a portion of a block move engine. Claim 12 provides similar limitations.

Chen appears silent regarding a number of the claimed elements. For example, Chen seems silent regarding an input signal received a scan line at a time, as presently claimed. No instance of scan lines in Chen has been cited. The words "scan" and "lines" are not found in Chen.

Furthermore, Chen is silent regarding a first circuit configured to scale and filter the input signal, as presently claimed. While the alpha blending may be a form of filtering, no citation has been provided for scaling. Furthermore, Applicant's representative points out that Chen clearly states that scaling operations are preferably handled in software, running in the host CPU 303 (see Col. 5, lines 49-50 of Chen). Therefore, Chen does not disclose **a first circuit** that filters and scales the input signal, as presently claimed.

Also, since the Examiner states (top of page 8) that the CPU 303 of Chen is considered to be the microprocessor coupled to the second circuit through a bus (as in presently pending claim 22), Chen appears silent regarding a **first circuit** configured to

scale and filter the input signal. Furthermore, previously presented claim 5, now incorporated into independent claim 1, provides that the apparatus comprises a portion of a block move engine. A first circuit and a second circuit, as part of the block move engine, where the first circuit is configured to scale and filter an input signal, where an input signal is received as a scan line at a time, is clearly not presented in Chen. Furthermore, such a block move engine that has a second circuit coupled to a microprocessor through a bus, as in claim 22, is clearly not shown in Chen. While Chen may use several words of the claimed invention, anticipation requires the presence, in a single prior art reference, the disclosure of **each and every element** of the claimed invention, **arranged as in the claim** (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(emphasis added by Applicants' representative). As pointed out, this standard has not been met.

As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

The rejection of claims 13-21 under 35 U.S.C. §102(b) as being anticipated by Bilbrey is respectfully traversed and should be withdrawn.

Bilbrey discloses a programmable digital video processing system (Title).

In contrast, claim 13 of the present invention provides a method for scaling and filtering of video, comprising the steps of (A) calculating an output signal having a first resolution and a plurality of output pixels in response to (i) an input signal having a second resolution and a plurality of input pixels and (ii) one or more control signals, (B) generating said control signals in response to (i) a previous calculation by step (A) and (ii) one or more input parameters, and (C) scaling and filtering said input signal to allow one or more of said input pixels to contribute to the creation of one or more of said output pixels. The input signal is received a single scan line at a time. The method is implemented in a block move engine.

Bilbrey appears silent regarding a number of the claimed elements. For example, Bilbrey seems silent regarding an input signal received a single scan line at a time, as presently claimed. At best, although still not clear in the Office Action, Bilbrey receives a capture input through the three inputs 68. However, such an input is analog, which is not received a single scan line at a time and does not comprise a plurality of input pixels, as presently claimed (see Appendix A). Bilbrey consistently describes these signals as "the three analog signals" (see column 5, lines 5-6). The signals are received and processed prior to the A/D

converter circuit 70. Prior to the circuit 70, the signals remain analog signals. One skilled in the art would understand that analog signals do not comprise a plurality of input pixels received as a single scan line, as presently claimed. As such, Bilbrey is silent regarding the claimed input signal comprising a plurality of input pixels. Bilbrey is also silent regarding a block move engine (BME), as presently claimed. As such, claim 1 is fully patentable over Bilbrey and the rejection should be withdrawn.

As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 4, 7 and 8 under 35 U.S.C. §103 is respectfully traversed and should be withdrawn. Claims 4, 7 and 8 depend, directly or indirectly, from the independent claims which are now believed to be allowable.

Regarding claim 4, Applicant's representative traverses the Examiner's suggestion that it is inherent that Chen reads on the claimed invention. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988).

FINALITY OF THE OFFICE ACTION

Applicant's representative respectfully requests reconsideration of the finality of the February 5, 2003 Office Action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

MPEP §706.07 further states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. They **must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal** unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

As discussed, since the Examiner failed to present arguments addressing elements of the claimed invention, a reconsideration of the finality is appropriate.

As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

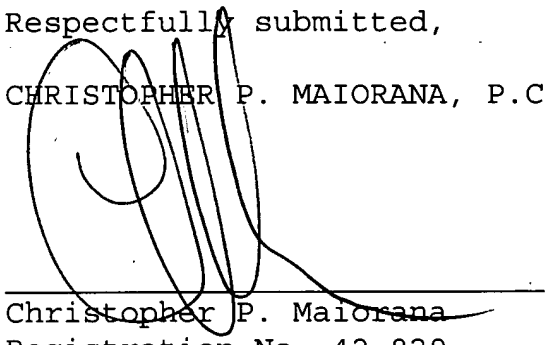
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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